**Experiment-7 : 4:1 Multiplexer**

**Objective:**

To design a 4:1 multiplexer and write a self-checking test bench that takes stimuli from a stored file stimuli.txt. The test bench should check the generated output with expected output and prints pass/fail messages.

**Tool Used:**

Xilinx ISE.

**Theory:**

fopen, foef, fscanf opens and reads the file for the written inputs. They are predefined functions to read the text file.

**DUT Code:**

module mux(input [3:0]i, [1:0]s, output y);

    assign y = s[1]?(s[0]?i[3]:i[2]):(s[0]?i[1]:i[0]);

endmodule

**TB Code:**

module tb;

    reg [3:0] i;// Inputs

    reg [1:0] s;

    wire y;

    integer A,C,fx ;

    reg [3:0] vector;

    mux uut (i, s, y); // Instantiate the Unit Under Test (UUT)

    initial begin

    vector = 3;

        fx = $fopen("C:\\Users\\User\\Documents\\input\_test.txt","r");

      while (! $feof(fx)) begin

         $fscanf(fx,"%b\t",A);

            i = A;

                $fscanf(fx,"%b\t",A);

            s = A;

                $fscanf(fx,"%b\t",A);

            C = A;

            #2;

            if (C == y)begin

                $display("success");

                     $display("value of i = %b, value of s = %b, output is %b",i,s,y);

             end

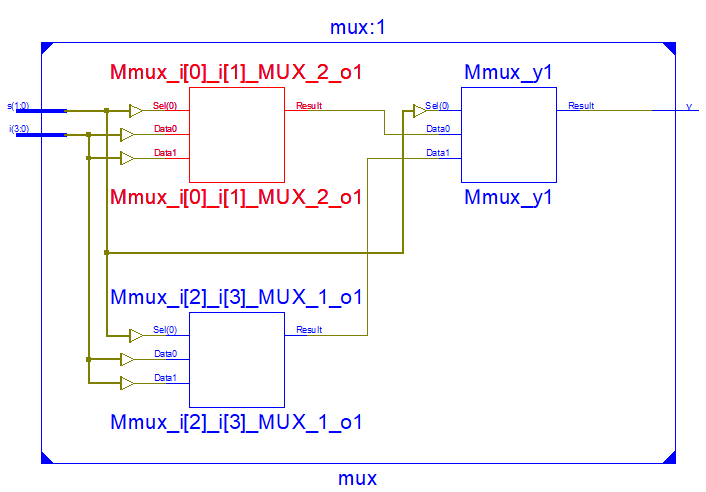
        end

        $fclose(fx);

    end

endmodule

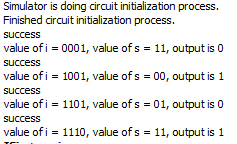
**RTL Diagram:**

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**Output Waveform:**

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**Simulation Output:**

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**Result:**

The simulation output and the RTL diagram is observed and found to be valid.